

AMENDMENTS TO THE DRAWINGS

The Transmittal of Formal Drawings (filed concurrently herewith) includes changes to Figures 3, 4 and 6. These sheets replace the original sheets including Figures 3, 4 and 6.

Figures 3 and 4 include non handwritten characters as requested by the Examiner. Figure 4 also includes reference numbers "404-410" and "412-438." A new figure 6 which corresponds to the Specification is also included.

REMARKS

Claims 1-18 are pending in the application. Claims 1 and 17 have been amended.

Applicants believe that this response addresses the Examiner's rejection and that any changes do not introduce new matter into the specification, limit the scope of the claims or result in any prosecution history estoppel.

Drawings

The Examiner objected to Figs. 3 and 4 for including handwritten characters. The Examiner also objected to Figure for not including reference signs mentioned in the description "404-410" and "412-430." Applicants respectfully note that new drawings including non handwritten characters are submitted with this response. A new Figure 4 including reference numbers "404-410" and "412-438" are included. A new Figure 6 which corresponds to the Specification is also included.

Specification

Regarding paragraph 1, related application numbers are provided. Regarding paragraph 33, line 7, "decision" symbol D is defined. Paragraph 33 has been amended to correspond the reference numerals to the rest of the Specification.

Claim Rejections – 35 USC S. 112

The Examiner rejected claims 1-6 and 12 under 35 USC S. 112, second paragraph, as being indefinite. Applicants note that claim 1 has been amended to recite "the a clean up pass." Claim 12 has been amended to recite "the a processor's register set."

Claim Rejections – 35 USC S. 102

The Examiner stated that the rejections of claims 1-18 under 35 U.S.C. 102(e) as being anticipated by Taubman. Applicants respectfully traverse the Examiner's rejection. In particular, all of the references, either alone or in combination, fail to teach or suggest "identify state variables associated with horizontal and vertical neighboring bits of the selected bits to be processed, determine whether state variables associated with coefficients bits and neighboring bits are zero, and in response to state variables associated with coefficient bits and neighboring bits being all zero, select run length coding" as claimed or similarly claimed.

As noted in the specification on page 8, paragraph [0034] to page 9, paragraph [0037]:

[0034] FIG. 4 is a block diagram of an embodiment 400 of register 402 for state variable sigma. In particular, the state variable is shown aligned in a processor's register set. The array of state variable sigmas corresponds to an array of quantized coefficients being scanned. **Each bit-plane of a code block is scanned in a particular order. Starting at the top left, the first four bit symbols of the column are scanned. Then the first four bit symbols of the second column, until the width of the code-block has been covered. Then the second four bit symbols of the first column are scanned and so on. A similar scan is continued for any leftover rows on the lowest code blocks in the sub-band. Sigma bits are typically stored in local processors registers in the same scan order as shown in FIG. 4. These can be shifted to the left to perform the same compare on the next scan.**

[0035] **Embodiments of the instruction will determine whether zero coding or run length coding should be implemented based upon the significance state variable sigmas of selected coefficient bits 404-410 and immediate horizontal and vertical neighboring bits 412-438. If they are zero, then run length coding is performed else zero coding is performed. The instruction is expanded to include NxM zero checks but in example the zero check is 3X6. This check is preferably performed on every 4 pixels and in every bit plane.**

[0036] The zero coding or run length coding decision according to the presently preferred embodiment of the invention may be implemented in response to an instruction set including decision instruction. When implementing this instruction, the host processor controls (either directly or indirectly) the zero coding or run length coding decision. In general, the exact operation sequence to be performed is based on the contents of the block master data structure, which contains the information of the current coefficient block which is being processed. The block master data structure can be implemented in either software or hardware, depending on the embodiment. In the presently preferred embodiments, the block master data structure is implemented as hardware, specifically, as a register set. The registers may include a sigma state variable registers which

contains the quantized coefficient values of the stripe currently being scanned and significance values. This register can be connected directly with the memory storage containing the coefficient values, or updated under control of the host processor. During encoding, this register may be scanned to produce the information required to control the operation sequences in the codec.

[0037] In a typical implementation, if the scanning block is 64 pixels by 64 pixels and each pixel is 16 bits, then this check must be performed $64/4 \times 64 \times 15 = 15360$ times. **Embodiments of the invention reduce the number of instruction it would take to check 18 bits for all zeros.** With current instructions, the processor typically reads row one and perform an AND to mask out all but 3 bits, then check for a zero flag. If zero flag, then read the next row, perform an AND, check the zero flag and so on. Thus, with two instructions per row times 6 rows = 12 instructions. Embodiments of the invention provide an instruction that is 12 times faster saving $11 \times 15360 = 168960$ instructions for just a 64 by 64 pixel block. (Emphasis added.)

Additionally, as noted in the specification on pages 10-11, paragraphs [0043] – [0046]:

[0043] In step 604, state variables associated with horizontal and vertical neighboring bits of the selected bits to be processed are identified.

[0044] In step 606, it is determined whether state variables associated with coefficients bits and neighboring bits are zero.

[0045] In response to state variables associated with coefficient bits and neighboring bits being all zero (step 606), run length coding is selected (step 608).

[0046] In response to at least one state variable associated with coefficient bits and neighboring bits being non-zero (step 606), zero coding is selected (step 610).

Taubman fails to teach or suggest “identify state variables associated with horizontal and vertical neighboring bits of the selected bits to be processed, determine whether state variables associated with coefficients bits and neighboring bits are zero, and in response to state variables associated with coefficient bits and neighboring bits being all zero, select run length coding.” Rather, Taubman is directed at four consecutive samples, not neighboring bits, having a zero state variable. For example, Taubman refers to on column 9, line 65 to column 10, line 12:

The Run-Lenght Coding operation is used in conjunction with the Zero Coding operation to reduce the average number of binary symbols that are encoded using the arithmetic coding engine. The RLC operation is invoked in place of the ZC operation if and only if the following conditions hold:

- (a) **Four consecutive samples have a zero state variable (i.e., $\sigma[m,n]=0$).**
- (b) **All four samples are identically zero neighborhoods. That is, the ZC neighborhood context variables, h , v , d and f is 0 for each of the four consecutive samples.**
- (c) All four samples are horizontally adjacent and reside within the same sub-block.
- (d) The group of four samples is aligned on a two-sample boundary. That is, proper groups of four samples start at the 1st, 3rd, 5th . . . sample of the relevant sub-block line.

All references are to the four consecutive samples, not neighboring bits, having a zero state variable. Taubman clarifies that the identically zero neighborhoods is referring to each of four consecutive samples themselves, not the adjacent samples.

CONCLUSION

In view of the foregoing, it is respectfully asserted that all of the claims pending in this patent application are in condition for allowance.

The required fee for a two month extension of time is enclosed. No additional fees are required for additional claims. Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666.

If the Examiner has any questions, he is invited to contact the undersigned at (323) 654-8218. Reconsideration of this patent application and early allowance of all the claims is respectfully requested.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on May 17, 2005.


Margaux Rodriguez

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